Remarks

The Office Action mailed July 17, 2006 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 26-29 are now pending in this application. Claims 26, 28, and 29 have been rejected. Claim 27 is withdrawn. Claims 1-25 are canceled without prejudice.

Applicant notes the assertion on page 4 of the Office Action that "Applicant's arguments with respect to the claims of record have been considered but are moot in view of the new ground(s) of rejection"; however the Office Action has not provided new grounds for rejection. Moreover, the Office Action has not provided any reasoning for the rejection of the Applicant's previously amended claims.

The rejection of Claim 26 under 35 U.S.C. § 103(a) as being unpatentable over Biard (U.S. Patent No. 4,661,726) is respectfully traversed.

Biard describes a buffered FET logic (BFL) gate. The BFL gate includes a plurality of transistors (32, 33, 36, and 37, Figure 4). The transistors (32, 33, and 36) are designed to have twice the width of the transistor (37) to provide equal positive and negative slew rates for charging a wiring capacitance on an output node.

Notably, in contrast to the present invention, Biard does not describe, suggest, or illustrate an output at an electrical node between a voltage drop circuit and a first channel and an output at an electrical node between a voltage drop circuit and a second channel. Rather, in contrast to the present invention **Biard merely describes a single output at an electrical node between a voltage drop and a second channel**. In contrast to the assertion on page 2 of the Office Action that "the node between element 32 and 33 forms a first output", **Figure 4 does not illustrate either a node nor an output between elements 32 and 33**. Furthermore, Biard never describes nor suggests a node or an output between elements 32 and 33. As such, the BFL gate described in Biard **cannot** provide a first output configured to provide a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit, and a second output configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit. Rather, Biard describes a BFL gate including a plurality of

transistors that provide equal positive and negative slew rates for charging a wiring capacitance at a **single output node**.

Claim 26 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an inverter stage input; an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output; a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel; a first output at an electrical node between said voltage drop circuit and said first channel, wherein said circuit is fabricated on a silicon carbide substrate; and a second output at an electrical node between said voltage drop circuit and said second channel, wherein said second output is configured to provide a first signal to a circuit other than said BFL level-shifting/inverter circuit, said first output is configured to provide a level-shifted signal to a circuit other than said BFL level-shifting/inverter circuit, and wherein the level-shifted signal is generated by shifting a voltage level of the first signal."

Biard does not describe nor suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit as recited in Claim 26. Specifically, Biard does not describe nor suggest a first output at an electrical node between the voltage drop circuit and the first channel, and a second output at an electrical node between the voltage drop circuit and the second channel, where the second output is configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit, the first output is configured to provide a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit, and where the level-shifted signal is generated by shifting a voltage level of the first signal. Rather, Biard describes a BFL gate including a plurality of transistors that provide equal positive and negative slew rates for charging a wiring capacitance **at a single output node**. Specifically, Biard does not describe nor suggest a second output that is configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit and a first output that is configured to provide a level-shifted signal to a circuit other than the BFL level-

shifting/inverter circuit. For the reasons set forth above, Claim 26 is submitted to be patentable over Biard.

In addition to the arguments set forth above, Applicant respectfully submits that the Section 103 rejection of Claim 26 as being unpatentable over Biard is not a proper rejection. As is well established, the mere assertion that it would have been obvious to one of ordinary skill in the art to have modified Biard to obtain the claimed recitations of the present invention does not support a prima facie obvious rejection. Rather, each allegation of what would have been an obvious matter of design choice must always be supported by citation to some reference work recognized as standard in the pertinent art and the Applicant given the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference. Applicant has not been provided with the citation to any reference supporting the combination made in the rejection. The rejection, therefore, fails to provide the Applicant with a fair opportunity to respond to the rejection, and fails to provide the Applicant with the opportunity to challenge the correctness of the rejection. Of course, such combinations are impermissible, and for this reason, along with the reasons set forth above, Applicant requests that the Section 103 rejection of Claim 26 be withdrawn.

The rejection of Claims 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Biard and further in view of Tohyama (U.S. Patent No. 4,810,907) and Alok et al. (U.S. Patent No. 6,559, 068) is respectfully traversed.

Biard is described above. Tohyama describes a level shift circuit. The circuit includes a plurality of metal semiconductor field effect transistors (MESFETs) (Q1 and Q2) with a resistor (R) between the MESFETs.

Alok et al. describe a method for improving inversion layer mobility in a silicon carbide metal-oxide semiconductor field-effect transistor (MOSFET) is provided. The method includes positioning a silicon carbide substrate and metallic impurities in a chamber, and forming an oxide layer on a surface of the silicon carbide substrate by introducing a gaseous mixture of hydrogen and oxygen into the chamber.

Claim 28 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an inverter stage input; an NMOS depletion

mode inverter responsive to said inverter stage input to produce an inverted output; a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel; and a resistor electrically connected in series between said first channel and said second channel; a first output at an electrical node between said resistor and said first channel; and a second output at an electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate, wherein said second output is configured to provide a first signal to a circuit other than said BFL level-shifting/inverter circuit, said first output is configured to provide a level-shifted signal to a circuit other than said BFL level-shifting/inverter circuit, and wherein the level-shifted signal is generated by shifting a voltage level of the first signal."

None of Biard, Tohyama, nor Alok et al., considered alone or in combination, describe or suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit as recited in Claim 28. Specifically, none of Biard, Tohyama, nor Alok et al., considered alone or in combination, describe nor suggest a first output at an electrical node between the resistor and the first channel, and a second output at an electrical node between the resistor and the second channel, where the circuit is fabricated on a silicon carbide substrate, where the second output is configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit, the first output is configured to provide a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit, and where the level-shifted signal is generated by shifting a voltage level of the first signal. Rather, Biard describes a BFL gate including a plurality of transistors that provide equal positive and negative slew rates for charging a wiring capacitance at a single output node. Specifically, Biard does not describe nor suggest a second output that is configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit and a first output that is configured to provide a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit. Tohyama describes a level shift circuit including a plurality of metal semiconductor field effect transistors (MESFETs) with a resistor between the MESFETs, and Alok et al. describe a silicon carbide metal-oxide semiconductor field-

effect transistor. Accordingly, none of Biard, Tohyama, nor Alok et al., considered alone or in combination, describe nor suggest the second output that is configured to provide a first signal to a circuit other than the BFL level-shifting/inverter circuit, the first output that is configured to provide a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit, and the level-shifted signal that is generated by shifting a voltage level of the first signal. For the reasons set forth above, Claim 28 is submitted to be patentable over Biard and further in view of Tohyama and Alok et al.

Claim 29 depends from independent Claim 28. When the recitations of Claim 29 are considered in combination with the recitations of Claim 28, Applicant submits that dependent Claim 29 likewise is patentable over Biard and further in view of Tohyama and Alok et al.

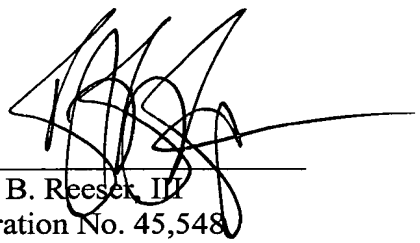
Moreover, Applicants respectfully submit that the Section 103 rejection of the presently pending claims is not a proper rejection. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Biard, Tohyama, nor Alok et al. considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to combine any one of Biard, Tohyama, and Alok et al. because there is no motivation to combine the references suggested in the art. Additionally, the Examiner has not pointed to any prior art that teaches or suggests to combine the disclosures, other than Applicants' own teaching.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejection is based on a combination of teachings selected in an attempt to arrive at the claimed invention. Since there is no teaching nor suggestion in the cited art for the combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for these reasons, along with the reasons given above, Applicants request that the Section 103 rejection of Claims 28 and 29 be withdrawn.

In view of the foregoing amendment and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



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